INFORMATION SOCIETY TECHNOLOGIES
(IST)
PROGRAMME

Contract for:

Concerted Action/Thematic Network

Final Report

Project acronym: ACiD-WG
Project full title: Working Group on Asynchronous Circuit Design
Contract no.: IST-1999-29119
Period: 1 September 2000 - 31 January 2005

Contents

1. Project summary

The European Commission funded the Working Group on Asynchronous Circuit Design (ACiD-WG) under the Fifth Framework Programme (FP5) Microelectronics, IST-1999-29119, for the period 1st September 2000 - 31st January 2005, and previously under FP3 Basic Research, EP7225, and FP4 Technologies for Components and Subsystems, EP21949.

Objectives for FP5

ACiD-WG aimed at **improving the systematic exchange of information and the forging of links between teams which carry out RTD or take-up activities around the theme of asynchronous circuit design**. Its objectives in FP5 were as follows:

1. **To encourage excellence in science and technology research pertaining to asynchronous circuits and systems.**
2. **To facilitate the development of methods and tools that are usable by engineers for the design of asynchronous VLSI systems.**
3. **To promote the adoption of asynchronous circuit design in industry.**

Description of the work during FP5

Four workshops were organised, hosted by members of the Working Group in different member and associated states of the European Union, on the theme of asynchronous circuits and systems. Attendance and presentations by all members of the Working Group and by industrial affiliates were encouraged. Invitations to participate were also extended to non-members of the Working Group. In addition, **visits between members took place and special interest group meetings were organised**.

A summer school and winter school were organised for the second year and fifth year of the contract, respectively. Members of the Working Group hosted these schools. **Additional teaching and training activities took place**. For example, ACiD-WG co-operated with the organisation of six-monthly meetings in the UK aimed at PhD students.

Members of the Working Group engaged in activities aimed at generating interest in and awareness of asynchronous circuits and systems, e.g., exploratory visits to companies, and tutorials at conferences. **They also disseminated the results of their research**, e.g., posters and presentations at conferences, and publication of books and journal articles. **Trip reports were produced and linked to the ACiD-WG website**, http://www.bcim.lsbu.ac.uk/ccsv/ACiD-WG/.

To demonstrate the strength of European RTD in asynchronous circuits and systems, participation in the annual ASYNC international symposium was considered particularly desirable.

A report "Design, Automation and Test for Asynchronous Circuits and Systems" was commissioned, which is of value to potential users of asynchronous circuit technology and to tools developers. **It was accompanied by an annual public overview of the status of asynchronous design in industrial use**.

2. Membership

Participant No.	*Short Name*	*Country Code*	*Type of Organisation*	*Date membership came into force*	*Date of termination*	*Requesting contribution from Commission*	*Representative on the Management Committee*
1	**LSBU**	UK	U	1/9/00		Yes	Mark Josephs (Chair)
2	**Philips Research**	NL	I	1/9/00		Yes	Ad Peeters
3	**Infineon**	D	I	1/9/00		Yes	Christoph Heer
4	**ST**	F	I	1/9/00		No	Jean-Pierre Schoellkopf
5	**CSEM**	S	R	1/9/00		No	Christian Piguet
6	**IHP**	D	R	1/9/00		Yes	Eckhard Grass
7	**MBDA**	UK	I	19/3/02		No	Eric Campbell
8	**UoM**	UK	U	1/9/00		Yes	Doug Edwards
9	**UNew**	UK	U	1/9/00		Yes	Alex Yakovlev
10	**UCam-CLab**	UK	U	1/9/00		Yes	Simon Moore
11	**UPC**	E	U	1/9/00		Yes	Jordi Cortadella
12	**UDI**	I	U	1/9/00	2/5/02	Yes	Luciano Lavagno
13	**TUE**	NL	U	1/9/00	5/4/03	Yes	Tom Verhoeff
14	**INPG-TIMA**	F	U	1/9/00		Yes	Marc Renaudin
15	**DTU**	DK	U	1/9/00		Yes	Jens Sparsø
16	**Technion**	IL	U	1/9/00		Yes	Ran Ginosar
17	**Åbo Akademi**	FIN	U	1/9/00		Yes	Kaisa Sere
18	**AT&T**	UK	I	1/9/00	24/4/02	No	Phil Endecott
19	**NNT**	IL	I	5/6/02	2/1/05	No	Victor Varshavsky (deceased)
20	**PoliTo**	I	U	2/5/02		Yes	Luciano Lavagno
21	**ICS-FORTH**	EL	U	2/5/02		Yes	Christos Sotiriou

U = University; R= Research Institute; I=Industrial organisation

The following companies became industrial affiliates of the Working Group:

- Accentime Inc, CA
- ARM Limited, UK
- Cadence Design Systems, US
- ExMark (Technical Marketing Services), UK
- Intel Corporation (Strategic CAD Labs), US
- Kramer-Consulting, DE
- Philips Semiconductors (Automotive), NL
- Sun Microsystems Laboratories (Asynchronous Design Group), US
- Theseus Logic, US

3. FP5 Sister Projects

ICS-FORTH, PoliTo and UoM participated in the project "Asynchronous open-source processor IP of the DLX architecture" (ASPIDA), IST-2002-37796, that aimed to demonstrate the feasibility of designing and delivering asynchronous Open Intellectual Property in a portable, re-usable manner.

UoM, UCam-CLab and INPG-TIMA participated in the project "Third generation Smart Card" (G3Card), IST-1999-13515, that explored the suitability of asynchronous logic in Smart Card processors as a means of increasing their robustness to attacks.

4. Workplan

The three objectives of ACiD-WG were met by following a workplan that consisted of four workpackages:

WP1 facilitated the systematic exchange and dissemination of information, and the forging of links between members of the Working Group and other parties. It was associated with six tasks and four deliverables.

WP2 was concerned with training measures that promote and support the dissemination, exploitation and enhancement of research knowledge. It was associated with two tasks and two deliverables.

WP3 produced reports that will help companies assess and evaluate asynchronous design. It was associated with two tasks and six deliverables.

WP4 was for project management. It was associated with five tasks and no deliverables.

WP1: Systematic exchange and dissemination of information

This workpackage was relevant to all three objectives. The organisation of four workshops by members of the Working Group were tasks that contributed to the systematic exchange and dissemination of information, and the forging of links between members of the Working Group and other participants. (The proceedings of each workshop were deliverables.) The organisation of two ASYNC symposia by members of the Working Group were tasks that facilitated participation by researchers from European industry and academic institutions. In addition, visits between members took place, special interest group meetings were organised, and members were represented at ASYNC symposia and other workshops and conferences.

Task	Date	Local Organiser	No. of Participants
ACiD-WG Workshop	12-13/2/01	CSEM	47
ACiD-WG Workshop	28-29/1/02	Infineon	71
ASYNC Symposium	8-11/4/02	UoM	118
ACiD-WG Workshop	27-28/1/03	ICS-FORTH	53
ASYNC Symposium	19-23/4/04	ICS-FORTH	93
ACiD-WG Workshop	28-29/6/04	Åbo Akademi	42

WP2: Training

This workpackage was relevant to the third objective. The organisation of a summer school and a winter school were tasks that resulted in the training of university students, young researchers and practising engineers in asynchronous circuit design. (The lecture notes of each school were collated as deliverables.) In addition, ACiD-

WG co-operated with the organisation of six-monthly meetings in the UK aimed at PhD students, and members gave tutorials and training courses.

Task	Date	Local Organiser	No. of Participants
ACiD-WG School	15-19/7/02	INPG-TIMA	90
ACiD-WG School	3-7/1/05	UCam-CLab	61

WP3: Assessment and evaluation

This workpackage was relevant to the second and third objectives. The ACiD-WG Management Committee undertook the task of reviewing the preliminary version of the commissioned report on design, automation and test for asynchronous circuits and systems (a deliverable) before a revised version (another deliverable) was made public. Members and industrial affiliates also had the task of contributing to annual updates and an annual overview of the status of asynchronous design in industry (further deliverables). These deliverables were prepared by Manchester Informatics Limited (which is associated with UoM).

WP4: Project management

The management committee met after each workshop and otherwise carried out business by electronic mail. The five periodic progress reports were tasks.

Deliverables list

Deliverable name	WP no.	Distribution	Delivery (project month)
Proceedings of 1st workshop	WP1	Public[1,2]	12
Proceedings of 2nd workshop	WP1	Public[1,2]	24
Proceedings of 3rd workshop	WP1	Public[1,2]	36
Proceedings of 4th workshop	WP1	Public[1,2]	48
Lecture notes from summer school	WP2	Restricted[1]	24
Lecture notes from winter school	WP2	Restricted[1]	53
Preliminary version of report on design, automation and test	WP3	Internal	6
Revised version of report	WP3	Public[1]	10
Initial overview of status of asynchronous design in industry	WP3	Public[1]	12
1st edition of report and overview	WP3	Public[1]	24
2nd edition of report and overview	WP3	Public[1,3]	36
3rd edition of report and overview	WP3	Public[1,2]	48

[1] Printed collections distributed to attendees at ACiD-WG workshops/schools, ACiD-WG members and industrial affiliates, Commission Project Officer and Reviewer.
[2] Linked to http://www.bcim.lsbu.ac.uk/ccsv/ACiD-WG/.
[3] Printed collections also distributed at DATE, Munich, 2003.

Evidence of success in Objective 1: "To encourage excellence in science and technology research pertaining to asynchronous circuits and systems."

Representative on the Management Committee	**Number of Publications listed by DBLP 23/04/05**					
	2005	**2004**	**2003**	**2002**	**2001**	**Total**
Campbell (MBDA)	0	0	0	0	0	**0**
Cortadella (UPC)	0	9	3	9	3	**24**
Edwards (UoM)	0	2	1	2	0	**5**
Ginosar (Technion)	0	3	2	0	0	**5**
Grass (IHP)	0	1	1	1	1	**4**
Heer (Infineon)	0	1	1	0	0	**2**
Josephs (LSBU)	0	3	1	2	0	**6**
Lavagno (PoliTo)	1	7	8	12	6	**34**
Moore (UCam-CLab)	0	2	1	3	1	**7**
Peeters (Philips Research)	0	1	1	5	3	**10**
Piguet (CSEM)	0	6	1	3	1	**11**
Renaudin (INPG-TIMA)	0	4	5	5	2	**16**
Schoellkopf (ST)	0	0	1	0	0	**1**
Sere (Åbo Akademi)	1	3	2	2	2	**10**
Sotiriou (ICS-FORTH)	0	5	1	1	0	**7**
Sparsø (DTU)	0	2	0	1	0	**3**
Varshavsky (NNT)	0	0	1	2	1	**4**
Yakovlev (UNew)	1	8	6	11	2	**28**
Total (less duplicates)	**3**	**48**	**34**	**55**	**21**	**161**

Notes

- DBLP is a comprehensive Computer Science Bibliography. See Appendix 1 for the full list of publications.
- Academic publication was not necessarily expected of representatives working in industry.
- Some of the articles counted above, especially among those authored by Lavagno and Sere, are not in the area of asynchronous circuit design.
- Other scientists affiliated to members of ACiD-WG have published in the area independently of the above representatives. In particular, Furber (who leads the group at UoM) has published for the most part independently of Edwards. His articles have not been counted above, though they have been listed at the end of Appendix 1.

	Number of ASYNC Publications					
Member	**2005**	**2004**	**2003**	**2002**	**2001**	**Total**
LSBU	0	0	1	0	0	**1**
Philips Research	2	0	0	2	2	**6**
Infineon	0	0	0	0	0	**0**
ST	1	0	0	0	1	**2**
CSEM	0	0	0	0	0	**0**
IHP	1	0	0	1	0	**2**
MBDA	0	0	0	0	0	**0**
UoM	0	1	3	1	4	**9**
UNew	0	0	2	2	1	**5**
UCam-CLab	1	1	0	2	0	**4**
UPC	0	1	0	0	1	**2**
INPG-TIMA	1	1	1	0	0	**3**
DTU	1	0	0	0	0	**1**
Technion	1	1	2	0	0	**4**
Åbo Akademi	0	0	0	0	0	**0**
NNT	0	0	0	0	0	**0**
PoliTo	0	1	0	0	0	**1**
ICS-FORTH	1	2	0	0	0	**3**
Total (less duplicates)	**8**	**5**	**9**	**8**	**8**	**38**
Submissions	61	60	66	43	43	**273**
Accepted	20	21	21	21	20	**103**

Notes

- ASYNC is the series of international symposia on asynchronous circuits and systems. See Appendix 2 for the full list of publications, with abstracts.
- The best paper awards in 2004 and 2005 went to members of ACiD-WG.
- The 2004 programme also included a keynote address by Philips Research and an invited talk on “12 Years of Support from the European Commission” by LSBU.

Evidence of success in Objective 2: "To facilitate the development of methods and tools which are usable by engineers for the design of asynchronous VLSI systems."

The following entries by members of ACiD-WG are listed in the report "Design, Automation and Test for Asynchronous Circuits and Systems", 3rd Edition, June 2004, http://www.bcim.lsbu.ac.uk/ccsv/ACiD-WG/AsyncToolSurvey.pdf.

Member	**Tools/Methodologies**
LSBU	di2pn, syndi and diana
Philips Research	Handshake Technology Design Flow*
Infineon	-
ST	-
CSEM	-
IHP	-
MBDA	Butler**
UoM	Balsa, LARD and Oolong
UNew	Clp, ConfRes, OptiMist, Punf, VeriMap and VerySAT
UCam-CLab	Veraci
UPC	Petrify*** and Transyt
INPG-TIMA	TAST
DTU	VSTGL
Technion	-
Åbo Akademi	-
NNT	-
PoliTo	Pipefitter
ICS-FORTH	-

* Handshake Technology is the semiconductor industry's first production proven methodology for using self-timed circuitry in commercial applications. Handshake Technology has been used for more than five years in tens of millions of products including smart cards, advanced pagers, In-Vehicle Network transceivers, and cordless handsets.

** A Queen's Awards for Enterprise 2004, in the Innovation category, http://www.queensawards.org.uk/business/Winners/2004.html#innovation, was conferred on MBDA for its development and industrial application of the "Butler Chip". The Butler Chip, developed at MBDA's Stevenage Research and Development facility for integration in advanced guided-weapon systems, provides hardware support to replace a conventional computer software operating system. Approximately half of this 460K-gate ASIC is clock-free circuitry.

*** The 2002 Descartes Prize Grand Jury selected the research work entitled "Petrify: Methodology and Tool for Logic Synthesis of Asynchronous Circuits", entered by Cortadella (UPC) in association with Lavagno (PoliTo), Yakovlev (UNew), Kishinevsky (Intel Corporation) and Kondratyev (Cadence Berkeley Laboratories), as one of the ten finalist projects, http://www.cordis.lu/science-society/descartes/finalists2002.htm.

Evidence of success in Objective 3: "To promote the adoption of asynchronous circuit design in industry."

Three members of ACiD-WG have introduced asynchronous circuit design into industrial practice. An overview of activities worldwide can be found in "The Status of Asynchronous Design in Industry", 3rd Edition, June 2004, http://www.bcim.lsbu.ac.uk/ccsv/ACiD-WG/AsyncIndustryStatus.pdf.

UoM

A number of post-doctoral researchers from Furber and Edward's group at UoM are now employed by **Silistix Limited**, a start-up company previously called Self-Timed Solutions. In December 2003, this UoM spin-out won its first round of venture capital, with Intel Capital as leading investor. Furber heads its Technical Advisory Committee. The company offers self-timed interconnect for linking standard synchronous IP blocks, so providing a low-power GALS (globally asynchronous, locally synchronous) solution to the timing-closure problem.

Philips Research

During 2003, the team from Philips Research founded a new Line of Business, **Handshake Solutions** (http://www.handshakesolutions.com), within the Technology Incubator. Peeters became Chief Technical Officer and Kessels became Senior Technology Consultant of the new company. Handshake Solutions sells products and services to both the semiconductor and electronics markets. Customers in these segments can range from small design houses to specialized device manufacturers and large semiconductor companies (including Philips Semiconductors).

In October 2004 Handshake Solutions and ARM announced the joint development and marketing of an asynchronous ARM® processor that will be particularly useful in the smart card, consumer electronics, and automotive markets because of its very low power consumption and low Electro Magnetic Interference (EMI). The processor will be available as a licensable core from ARM in Q1 2005 and will be supported by Handshake Solutions' advanced design tools and methodology that enables customers to design a complete or partially asynchronous chip. ARM has long recognised the potential of asynchronous design, supporting the AMULET research work at UoM.

MBDA

The Butler Chip is used within MBDA's new ASRAAM air-to-air missile, which since entering service with the Royal Air Force in 2002 has set the international benchmark for air combat weapons. ASRAAM's unmatched features, including exceptional speed, accuracy and rapid manoeuvrability, combine to make it the out and out leader in its class. The Butler Chip has also been integrated within the Royal Navy's Vertical Launch Seawolf naval air-defence system and will be a key technology in future guided weapons developed by the company.

There is also a wide range of potential applications for this kind of technology in non-defence related industry where real-time safety related mechanisms are called for. MBDA has already demonstrated the technology within the nose wheel steering system of a commercial airliner. The Butler Chip could also provide the answer to the inherent dangers posed by the movement of heavy autonomous robots within a modern factory environment.

Appendix 1 – Publications by Members' Representatives

The following articles were listed by dblp.uni-trier.de, the Computer Science Bibliography maintained by the University of Trier, when searched by author on 24 March 2005 using the name of the representative for each member of ACiD-WG.

Cortadella (UPC)

		2004
24		Jordi Cortadella, Wolfgang Reisig: Applications and Theory of Petri Nets 2004, 25th International Conference, ICATPN 2004, Bologna, Italy, June 21-25, 2004, Proceedings Springer 2004
23	EE	Robert Clarisó, Jordi Cortadella: Verification of timed circuits with symbolic delays. ASP-DAC 2004: 628-633
22	EE	Ivan Blunno, Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Kelvin Lwin, Christos P. Sotiriou: Handshake Protocols for De-Synchronization. ASYNC 2004: 149-158
21	EE	David Bañeres, Jordi Cortadella, Michael Kishinevsky: A recursive paradigm to solve Boolean relations. DAC 2004: 416-421
20	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Kelvin Lwin, Christos P. Sotiriou: From Synchronous to Asynchronous: An Automatic Approach. DATE 2004: 1368-1369
19	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Christos P. Sotiriou: Coping with The Variability of Combinational Logic Delays. ICCD 2004: 505-508
18	EE	Robert Clarisó, Jordi Cortadella: The Octahedron Abstract Domain. SAS 2004: 312-327
17	EE	Peter A. Beerel, Jordi Cortadella, Alex Kondratyev: Bridging the Gap between Asynchronous Design and Designers. VLSI Design 2004: 18-20
16	EE	Nilesh Modi, Jordi Cortadella: Boolean Decomposition Using Two-literal Divisors. VLSI Design 2004: 765-768
		2003
15	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Yosinori Watanabe: Quasi-Static Scheduling for Concurrent Architectures. ACSD 2003: 29-40
14	EE	Josep Carmona, Jordi Cortadella: ILP Models for the Synthesis of Asynchronous Control Circuits. ICCAD 2003: 818-826
13	EE	Josep Carmona, Jordi Cortadella, Victor Khomenko, Alexandre Yakovlev: Synthesis of Asynchronous Hardware from Petri Nets. Lectures on Concurrency and Petri Nets 2003: 345-401
		2002
12		Jordi Cortadella, Alexandre Yakovlev, Grzegorz Rozenberg: Concurrency and Hardware Design, Advances in Petri Nets Springer 2002
11	EE	Jordi Cortadella, Alexandre Yakovlev, Jim D. Garside: T8: Logic Design of Asynchronous Circuits. ASP-DAC 2002: 26-30
10	EE	Josep Carmona, Jordi Cortadella, Enric Pastor: Synthesis of Reactive Systems: Application to Asynchronous Circuit Design. Concurrency and Hardware

		Design 2002: 108-151
9	EE	Marco A. Peña, Jordi Cortadella, Alexander B. Smirnov, Enric Pastor: A Case Study for the Verification of Complex Timed Circuits: IPCMOS. DATE 2002: 44-53
8	EE	Josep Carmona, Jordi Cortadella: Input/Output Compatibility of Reactive Systems. FMCAD 2002: 360-377
7	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Claudio Passerone, Yosinori Watanabe: Quasi-Static Scheduling of Independent Tasks for Reactive Systems. ICATPN 2002: 80-100
6		Jordi Cortadella: Bi-Decomposition and Tree-Height Reduction for Timing Optimization. IWLS 2002: 233-238
5	EE	Jordi Cortadella, Alexandre Yakovlev, Jim D. Garside: Logic Design of Asynchronous Circuits (Tutorial Abstract). VLSI Design 2002: 26-
4		Josep Carmona, Jordi Cortadella, Enric Pastor: A structural encoding technique for the synthesis of asynchronous circuits. Fundam. Inform. 50(2): 135-154 (2002)
2001		
3	EE	Josep Carmona, Jordi Cortadella, Enric Pastor: A structural encoding technique for the synthesis of asynchronous circuits. ACSD 2001: 157-166
2	EE	Gianluca Cornetta, Jordi Cortadella: A Multi-Radix Approach to Asynchronous Division. ASYNC 2001: 25-
1	EE	Enric Pastor, Jordi Cortadella, Oriol Roig: Symbolic Analysis of Bounded Petri Nets. IEEE Trans. Computers 50(5): 432-448 (2001)

Edwards (UoM)

2004		
5	EE	Aristides Efthymiou, John Bainbridge, Douglas A. Edwards: Adding Testability to an Asynchronous Interconnect for GALS SoC. Asian Test Symposium 2004: 20-23
4	EE	Aristides Efthymiou, Christos P. Sotiriou, Douglas A. Edwards: Automatic Scan Insertion and Pattern Generation for Asynchronous Circuits. DATE 2004: 672-673
2003		
3	EE	W. J. Bainbridge, W. B. Toms, Doug Edwards, Stephen B. Furber: Delay-Insensitive, Point-to-Point Interconnect Using M-of-N Codes. ASYNC 2003: 132-140
2002		
2	EE	Tiberiu Chelcea, Steven M. Nowick, Andrew Bardsley, Doug Edwards: A Burst-Mode Oriented Back-End for the Balsa Synthesis System. DATE 2002: 330-337
1	EE	Doug Edwards, Andrew Bardsley: Balsa: An Asynchronous Hardware Synthesis Language. Comput. J. 45(1): 12-18 (2002)

Ginosar (Technion)

		2004
5	EE	Rostislav (Reuven) Dobkin, Ran Ginosar, Christos P. Sotiriou: Data Synchronization Issues in GALS SoCs. ASYNC 2004: 170-180
4	EE	Alex Branover, Rakefet Kol, Ran Ginosar: Asynchronous Design By Conversion: Converting Synchronous Circuits into Asynchronous Ones. DATE 2004: 870-877
3	EE	Uri Frank, Ran Ginosar: A Predictive Synchronizer for Periodic Clock Domains. PATMOS 2004: 402-412
		2003
2	EE	Yaron Semiat, Ran Ginosar: Timing Measurements of Synchronization Circuits. ASYNC 2003: 68-77
1	EE	Ran Ginosar: Fourteen Ways to Fool Your Synchronizer. ASYNC 2003: 89-97

Grass (IHP)

		2004
4	EE	Milos Krstic, Eckhard Grass: GALSification of IEEE 802.11a Baseband Processor. PATMOS 2004: 258-267
		2003
3	EE	Milos Krstic, Eckhard Grass: New GALS Technique for Datapath Architectures. PATMOS 2003: 161-170
		2002
2	EE	Eckhard Grass, Bodhisatya Sarker, Koushik Maharatna: A Dual-Mode Synchronous/Asynchronous CORDIC Processor. ASYNC 2002: 76-83
		2001
1	EE	V. A. Bartlett, Eckhard Grass: A Low-Power Asynchronous VLSI FIR Filter. ARVLSI 2001: 29-41

Heer (Infineon)

		2004
2	EE	Christian Piguet, Jacques Gautier, Christoph Heer, Ian O'Connor, Ulf Schlichtmann: Extremely Low-Power Logic. DATE 2004: 656-663
		2003
1	EE	Tim Schoenauer, Jörg Berthold, Christoph Heer: Reduced Leverage of Dual Supply voltages in Ultra Deep Submicron Technologies. PATMOS 2003: 41-50

Josephs (LSBU)

		2004
6	EE	Hemangee K. Kapoor, Mark B. Josephs, Dennis P. Furey: Verification and Implementation of Delay-Insensitive Processes in Restrictive Environments. ACSD 2004: 89-98
5	EE	Hemangee K. Kapoor, Mark B. Josephs: Decomposing specifications with

		concurrent outputs to resolve state coding conflicts in asynchronous logic synthesis. DAC 2004: 830-833
4	EE	Hemangee K. Kapoor, Mark B. Josephs: Modelling and verification of delay-insensitive circuits using CCS and the Concurrency Workbench. Inf. Process. Lett. 89(6): 293-296 (2004)
		2003
3	EE	Mark B. Josephs: An Analysis of Determinacy Using a Trace-Theoretic Model of Asynchronous Circuits. ASYNC 2003: 121-131
		2002
2	EE	Mark B. Josephs, Dennis P. Furey: A Programming Approach to the Design of Asynchronous Logic Blocks. Concurrency and Hardware Design 2002: 34-60
1	EE	Igor Lemberski, Mark B. Josephs: Optimal Two-Level Delay - Insensitive Implementation of Logic Functions. PATMOS 2002: 92-100

Lavagno (PoliTo)

		2005
34		Luciano Lavagno, Claudio Passerone: Design of Embedded Systems. The Industrial Information Technology Handbook 2005: 1-14
		2004
33	EE	Ivan Blunno, Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Kelvin Lwin, Christos P. Sotiriou: Handshake Protocols for De-Synchronization. ASYNC 2004: 149-158
32	EE	Alberto La Rosa, Claudio Passerone, Francesco Gregoretti, Luciano Lavagno: Implementation of a UMTS Turbo-Decoder on a Dynamically Reconfigurable Platform. DATE 2004: 1218-1223
31	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Kelvin Lwin, Christos P. Sotiriou: From Synchronous to Asynchronous: An Automatic Approach. DATE 2004: 1368-1369
30	EE	Jean-Yves Brunel, Marco Di Natale, Alberto Ferrari, Paolo Giusto, Luciano Lavagno: SoftContract: an Assertion-Based Software Development Process that Enables Design-by-Contract. DATE 2004: 358-363
29	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Christos P. Sotiriou: Coping with The Variability of Combinational Logic Delays. ICCD 2004: 505-508
28	EE	Luciano Lavagno, Marco Di Natale, Alberto Ferrari, Paolo Giusto: SoftContract: Model-Based Design of Error-Checking Code and Property Monitors. UML Satellite Activities 2004: 150-162
27		Luciano Lavagno: DAC Highlights. IEEE Design & Test of Computers 21(3): 259-260 (2004)
		2003
26	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Yosinori Watanabe: Quasi-Static Scheduling for Concurrent Architectures. ACSD 2003: 29-40
25	EE	Alberto La Rosa, Luciano Lavagno, Claudio Passerone: Hardware/Software

		Design Space Exploration for a Reconfigurable Processor. DATE 2003: 10570-10575
24	EE	Laura Vanzago, Bishnupriya Bhattacharya, Joel Cambonie, Luciano Lavagno: Design Space Exploration for a Wireless Protocol on a Reconfigurable Platform. DATE 2003: 10662-10667
23	EE	Fabio Campi, Andrea Cappelli, Roberto Guerrieri, Andrea Lodi, Mario Toma, Alberto La Rosa, Luciano Lavagno, Claudio Passerone, Roberto Canegallo: A Reconfigurable Processor Architecture and Software Development Environment for Embedded Systems. IPDPS 2003: 171
22	EE	Gianpiero Cabodi, Sergio Nocco, Stefano Quer, Alex Kondratiev, Luciano Lavagno, Yosinori Watanabe: A BMC-formulation for the scheduling problem in highly constrained hardware Systems. Electr. Notes Theor. Comput. Sci. 89(4): (2003)
21	EE	Felice Balarin, Yosinori Watanabe, Harry Hsieh, Luciano Lavagno, Claudio Passerone, Alberto L. Sangiovanni-Vincentelli: Metropolis: An Integrated Electronic System Design Environment. IEEE Computer 36(4): 45-52 (2003)
20		Luciano Lavagno, Limor Fix: DAC Highlights. IEEE Design & Test of Computers 20(3): 88-89 (2003)
19	EE	Alberto L. Sangiovanni-Vincentelli, Luciano Lavagno: Guest Editors' Introduction: Trends and Directions in Microelectronics. IEEE Micro 23(3): 6-7 (2003)
		2002
18	EE	Luciano Lavagno, Sujit Dey, Rajesh Gupta: Specification, Modeling and Design Tools for System-on-Chip. ASP-DAC 2002: 21-23
17	EE	Felice Balarin, Luciano Lavagno, Claudio Passerone, Alberto L. Sangiovanni-Vincentelli, Yosinori Watanabe, Guang Yang: Concurrent execution semantics and sequential simulation algorithms for the metropolis meta-model. CODES 2002: 13-18
16	EE	Felice Balarin, Luciano Lavagno, Claudio Passerone, Alberto L. Sangiovanni-Vincentelli, Marco Sgroi, Yosinori Watanabe: Modeling and Designing Heterogeneous Systems. Concurrency and Hardware Design 2002: 228-273
15	EE	G. Arrigoni, L. Duchini, Claudio Passerone, Luciano Lavagno, Yosinori Watanabe: False Path Elimination in Quasi-Static Scheduling. DATE 2002: 964-970
14	EE	Felice Balarin, Luciano Lavagno, Claudio Passerone, Yosinori Watanabe: Processes, Interfaces and Platforms. Embedded Software Modeling in Metropolis. EMSOFT 2002: 407-416
13	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Claudio Passerone, Yosinori Watanabe: Quasi-Static Scheduling of Independent Tasks for Reactive Systems. ICATPN 2002: 80-100
12	EE	Paolo Giusto, Jean-Yves Brunel, Alberto Ferrari, Eliane Fourgeau, Luciano Lavagno, Alberto L. Sangiovanni-Vincentelli: Automotive Virtual Integration Platforms: Why's, What's, and How's. ICCD 2002: 370-378
11	EE	Paolo Giusto, Jean-Yves Brunel, Alberto Ferrari, Eliane Fourgeau, Luciano Lavagno, Barry Orourke, Alberto L. Sangiovanni-Vincentelli, Emanuele Guasto:

		Models of IP's for Automotive Virtual Integration Platforms. ICCD 2002: 379-
10	EE	Ivan Blunno, Luciano Lavagno: Designing an Asynchronous Microcontroller Using Pipefitter. ICCD 2002: 488-493
9	EE	Luciano Lavagno, Mihai T. Lazarescu, Stefano Quer, Sergio Nocco, Claudio Passerone, Gianpiero Cabodi: A Symbolic Approach for the Combined Solution of Scheduling and Allocation. ISSS 2002: 237-242
8	EE	Luciano Lavagno, Sujit Dey, Rajesh K. Gupta: Specification, Modeling and Design Tools for System-on-Chip (Tutorial Abstract). VLSI Design 2002: 21-23
7	EE	Luciano Lavagno: Guest Editor's Introduction: Systems on a Chip--The Next Electronic Frontier. IEEE Micro 22(5): 14-15 (2002)
		2001
6	EE	Alberto La Rosa, Luciano Lavagno, Claudio Passerone: A software development tool chain for a reconfigurable processor. CASES 2001: 93-98
5	EE	André Châtelain, Yves Mathys, Giovanni Placido, Alberto La Rosa, Luciano Lavagno: High-level architectural co-simulation using Esterel and C. CODES 2001: 189-194
4	EE	Grant Martin, Luciano Lavagno, Jean Louis-Guerin: Embedded UML: a merger of real-time UML and co-design. CODES 2001: 23-28
3	EE	Leonardo Maria Reyneri, F. Cucinotta, A. Serra, Luciano Lavagno: A Hardware/Software Co-design Flow and IP Library Based of Simulink™. DAC 2001: 593-598
2	EE	Claudio Passerone, Yosinori Watanabe, Luciano Lavagno: Generation of minimal size code for scheduling graphs. DATE 2001: 668-673
1	EE	Radu Marculescu, Amit Nandi, Luciano Lavagno, Alberto L. Sangiovanni-Vincentelli: System-Level Power/Performance Analysis of Portable Multimedia Systems Communicating over Wireless Channels. ICCAD 2001: 207-

Moore (UCam-CLab)

		2004
7	EE	Robert D. Mullins, Andrew West, Simon Moore: Low-Latency Virtual-Channel Routers for On-Chip Networks. ISCA 2004: 188-197
6	EE	Scott Fairbanks, Simon W. Moore: Analog Micropipeline Rings for High Precision Timing. ASYNC 2004: 41-50
		2003
5	EE	Jacques J. A. Fournier, Simon Moore, Huiyun Li, Robert D. Mullins, George S. Taylor: Security Evaluation of Asynchronous Circuits. CHES 2003: 137-151
		2002
4	EE	Simon W. Moore, Robert D. Mullins, Paul A. Cunningham, Ross J. Anderson, George S. Taylor: Improving Smart Card Security Using Self-Timed Circuits. ASYNC 2002: 211-
3	EE	George S. Taylor, Simon W. Moore, Robert D. Mullins, Peter Robinson: Point to Point GALS Interconnect. ASYNC 2002: 69-75
2	EE	Panit Watcharawitch, Simon W. Moore: JMA: The Java-Multithreading

		Architecture for Embedded Processors. ICCD 2002: 527-
2001		
1	EE	Simon W. Moore: Protecting Consumer Security Devices. E-smart 2001: 1

Peeters (Philips Research)

2004		
10	EE	Ad M. G. Peeters: Bringing Handshake Technology to the Open Market. ASYNC 2004: 183
2003		
9	EE	Joep L. W. Kessels, Ad M. G. Peeters, Suk-Jin Kim: Bridging Clock Domains by Synchronizing the Mice in the Mousetrap. PATMOS 2003: 141-150
2002		
8	EE	Frank de Beest, Kees van Berkel, Ad M. G. Peeters: Adding Synchronous and LSSD Modes to Asynchronous Circuits. ASYNC 2002: 161-170
7	EE	Joep L. W. Kessels, Suk-Jin Kim, Ad M. G. Peeters, Paul Wielage: Clock Synchronization through Handshake Signalling. ASYNC 2002: 59-68
6	EE	Kees G. W. Goossens, Paul Wielage, Ad M. G. Peeters, Jef L. van Meerbergen: Networks on Silicon: Combining Best-Effort and Guaranteed Services. DATE 2002: 423-427
5	EE	Frank te Beest, Ad M. G. Peeters, Marc Verra, Kees van Berkel, Hans G. Kerkhoff: Automatic Scan Insertion and Test Generation for Asynchronous Circuits. ITC 2002: 804-813
4	EE	Francesco Pessolano, Joep L. W. Kessels, Ad M. G. Peeters: MDSP: A High-Performance Low-Power DSP Architecture. PATMOS 2002: 35-44
2001		
3	EE	Joep L. W. Kessels, Ad M. G. Peeters, Torsten Kramer, Markus Feuser, Klaus Ully: Designing an Asynchronous Bus Interface. ASYNC 2001: 108-117
2	EE	Ad M. G. Peeters, Kees van Berkel: Synchronous Handshake Circuits. ASYNC 2001: 86-95
1	EE	Joep Kessels, Ad Peeters: The tangram framework (embedded tutorial): asynchronous circuits for low power. ASP-DAC 2001: 255-260

Piguet (CSEM)

2004		
11	EE	Christian Piguet, Jacques Gautier, Christoph Heer, Ian O'Connor, Ulf Schlichtmann: Extremely Low-Power Logic. DATE 2004: 656-663
10	EE	Ingrid Verbauwhede, Patrick Schaumont, Christian Piguet, Bart Kienhuis: Architectures and Design Techniques for Energy Efficient Embedded DSP and Multimedia Processing. DATE 2004: 988-995
9	EE	Christian Schuster, Jean-Luc Nagel, Christian Piguet, Pierre-André Farine: Leakage Reduction at the Architectural Level and Its Application to 16 Bit Multiplier Architectures. PATMOS 2004: 169-178

8	EE	S. Cserveny, Jean-Marc Masgonty, Christian Piguet: Noise Margin in Low Power SRAM Cells. PATMOS 2004: 889-898
7		Christian Piguet, Narayanan Vijaykrishnan: Guest Editorial. IEEE Trans. VLSI Syst. 12(2): 129-130 (2004)
6		Christian Piguet, Narayanan Vijaykrishnan: Guest Editorial. IEEE Trans. VLSI Syst. 12(3): 233-234 (2004)
2003		
5	EE	S. Cservany, Jean-Marc Masgonty, Christian Piguet: Stand-by Power Reduction for Storage Circuits. PATMOS 2003: 229-238
2002		
4		Vivek De, Mary Jane Irwin, Ingrid Verbauwhede, Christian Piguet: Proceedings of the 2002 International Symposium on Low Power Electronics and Design, 2002, Monterey, California, USA, August 12-14, 2002 ACM 2002
3		Michel Robert, Bruno Rouzeyre, Christian Piguet, Marie-Lise Flottes: SOC Design Methodologies, IFIP TC10/WG10.5 Eleventh International Conference on Very Large Scale Integration of Systems-on/Chip (VLSI-SOC'01), December 3-5, 2001, Montpellier, France Kluwer 2002
2	EE	Christian Piguet: The First Quartz Electronic Watch. PATMOS 2002: 1-15
2001		
1	EE	Christian Piguet, Marc Renaudin, Thierry J.-F. Omnés: Low-power systems on chips (SOCs). DATE 2001: 488

Renaudin (INPG-TIMA)

2004		
16	EE	F. Aeschlimann, Emmanuel Allier, Laurent Fesquet, Marc Renaudin: Asynchronous FIR Filters: Towards a New Digital Processing Chain. ASYNC 2004: 198-206
15	EE	Marc Renaudin, F. Bouesse, Ph. Proust, J. P. Tual, L. Sourgen, F. Germain: High Security Smartcards. DATE 2004: 228-233
14	EE	Y. Monnet, Marc Renaudin, Régis Leveugle: Asynchronous Circuits Sensitivity to Fault Injection. IOLTS 2004: 121-128
13	EE	Kamel Slimani, Yann Rémond, Gilles Sicard, Marc Renaudin: TAST Profiler and Low Energy Asynchronous Design Methodology. PATMOS 2004: 268-277
2003		
12	EE	Emmanuel Allier, Gilles Sicard, Laurent Fesquet, Marc Renaudin: A New Class of Asynchronous A/D Converters Based on Time Quantization. ASYNC 2003: 196-205
11	EE	Dominique Borrione, Menouer Boubekeur, Emil Dumitrescu, Marc Renaudin, Jean-Baptiste Rigaud, Antoine Sirianni: An Approach to the Introduction of Formal Validation in an Asynchronous Circuit Design Flow. HICSS 2003: 279
10	EE	João Leonardo Fragoso, Gilles Sicard, Marc Renaudin: Power/Area Tradeoffs

		in 1-of-M Parallel-Prefix Asynchronous Adders. PATMOS 2003: 171-180
9	EE	Philippe Maurine, Jean-Baptiste Rigaud, F. Bouesse, Gilles Sicard, Marc Renaudin: Statistic Implementation of QDI Asynchronous Primitives. PATMOS 2003: 181-191
8		Dominique Borrione, Menouer Boubekeur, Laurent Mounier, Marc Renaudin, Antoine Sirianni: Validation of asynchronous circuit specifications using IF/CADP. VLSI-SOC 2003: 86-91
		2002
7	EE	Jean-Baptiste Rigaud, Laurent Fesquet, Marc Renaudin, Jerome Quartana: High-Level Modeling and Design of Asynchronous Arbiters for On-Chip Communication Systems. DATE 2002: 1090
6	EE	Quoc Thai Ho, Jean-Baptiste Rigaud, Laurent Fesquet, Marc Renaudin, Robin Rolland: Implementing Asynchronous Circuits on LUT Based FPGAs. FPL 2002: 36-46
5		Anh Vu Dihn Duc, Laurent Fesquet, Marc Renaudin: Synthesis of QDI Asynchronous Circuits from DTL-Style Petri-Net. IWLS 2002: 191-196
4	EE	Mohammed Es Salhiene, Laurent Fesquet, Marc Renaudin: Dynamic Voltage Scheduling for Real Time Asynchronous Systems. PATMOS 2002: 390-399
3	EE	Emmanuel Allier, Laurent Fesquet, Marc Renaudin, Gilles Sicard: Low-Power Asynchronous A/D Conversion. PATMOS 2002: 81-91
		2001
2	EE	Christian Piguet, Marc Renaudin, Thierry J.-F. Omnés: Low-power systems on chips (SOCs). DATE 2001: 488
1		Jean-Baptiste Rigaud, Jerome Quartana, Laurent Fesquet, Marc Renaudin: Modeling and Design of Asynchronous Priority Arbiters for On-Chip Communication Systems. VLSI-SOC 2001: 313-324

Schoellkopf (ST)

		2003
1	EE	Andrew B. Kahng, Shekhar Borkar, John Cohn, Antun Domic, Patrick Groeneveld, Louis Scheffer, Jean-Pierre Schoellkopf: Nanometer design: place your bets. DAC 2003: 546-547

Sere (Åbo Akademi)

		2005
10	EE	Juha Plosila, Kaisa Sere, Marina A. Waldén: Asynchronous system synthesis. Sci. Comput. Program. 55(1-3): 259-288 (2005)
		2004
9	EE	Lu Yan, Kaisa Sere, Xinrong Zhou, Jun Pang: Towards an Integrated Architecture for Peer-to-Peer and Ad Hoc Overlay Network Applications. FTDCS 2004: 312-318
8	EE	Lu Yan, Moisés Ferrer Serra, Guangcheng Niu, Xinrong Zhou, Kaisa Sere: SkyMin: A Massive Peer-to-Peer Storage System. GCC 2004: 527-534

7	EE	Lu Yan, Kaisa Sere: A Formalism for Context-Aware Mobile Computing. ISPDC/HeteroPar 2004: 14-21
		2003
6	EE	Lu Yan, Kaisa Sere: Stepwise Development of Peer-to-Peer Systems. IWFM 2003
5		Mauno Rönkkö, Anders P. Ravn, Kaisa Sere: Hybrid action systems. Theor. Comput. Sci. 290(1): 937-973 (2003)
		2002
4		Michael J. Butler, Luigia Petre, Kaisa Sere: Integrated Formal Methods, Third International Conference, IFM 2002, Turku, Finland, May 15-18, 2002, Proceedings Springer 2002
3	EE	Juha Plosila, Kaisa Sere, Marina A. Waldén: Design with Asynchronously Communicating Components. FMCO 2002: 424-442
		2001
2		Kaisa Sere, Wang Li: Guest Editors' Foreword. Nord. J. Comput. 8(1): 1 (2001)
1	EE	Kaisa Sere, Marina A. Waldén: Structuring and Verifying Distributed Algorithms. Nord. J. Comput. 8(2): 193-218 (2001)

Sotiriou (ICS-FORTH)

		2004
7	EE	Ivan Blunno, Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Kelvin Lwin, Christos P. Sotiriou: Handshake Protocols for De-Synchronization. ASYNC 2004: 149-158
6	EE	Rostislav (Reuven) Dobkin, Ran Ginosar, Christos P. Sotiriou: Data Synchronization Issues in GALS SoCs. ASYNC 2004: 170-180
5	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Kelvin Lwin, Christos P. Sotiriou: From Synchronous to Asynchronous: An Automatic Approach. DATE 2004: 1368-1369
4	EE	Aristides Efthymiou, Christos P. Sotiriou, Douglas A. Edwards: Automatic Scan Insertion and Pattern Generation for Asynchronous Circuits. DATE 2004: 672-673
3	EE	Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Christos P. Sotiriou: Coping with The Variability of Combinational Logic Delays. ICCD 2004: 505-508
		2003
2	EE	Manish Amde, Ivan Blunno, Christos P. Sotiriou: Automating the design of an asynchronous DLX microprocessor. DAC 2003: 502-507
		2002
1	EE	Christos P. Sotiriou: Implementing asynchronous circuits using a conventional EDA tool-flow. DAC 2002: 415-418

Sparsø (DTU)

2004		
3	EE	S. F. Nielsen, Jens Sparsø, J. Madsen: Towards Behavioral Synthesis of Asynchronous Circuits - An Implementation Template Targeting Syntax Directed Compilation. DSD 2004: 298-305
2	EE	T. Bjerregaard, S. Mahadevan, Jens Sparsø: A Channel Library for Asynchronous Circuit Design Supporting Mixed-Mode Modeling. PATMOS 2004: 301-310
2002		
1	EE	Vojin G. Oklobdzija, Jens Sparsø: Future directions in clocking multi-ghz systems. ISLPED 2002: 219

Varshavsky (NNT)

2003		
4	EE	Victor Varshavsky, Ilya Levin, Vladimir Ostrovsky: Increasing Implementability of beta-driven Threshold Checkers. IOLTS 2003: 158
2002		
3	EE	Victor Varshavsky, Vyacheslav Marakhovsky: GALA (Globally Asynchronous - Locally Arbitrary) Design. Concurrency and Hardware Design 2002: 61-107
2	EE	Victor Varshavsky, Vyacheslav Marakhovsky: GALA Approach in Design of Asynchronous Control for Counterflow Pipeline Processor. DELTA 2002: 73-80
2001		
1	EE	Victor Varshavsky, Vyacheslav Marakhovsky: A Neuron-MOS Threshold Element with Switching Capacitors. Fuzzy Days 2001: 430-435

Yakovlev (UNew)

2005		
28	EE	D. Koppad, Alexandre V. Bystrov, Alexandre Yakovlev: Off-Line Testing of Asynchronous Circuits. VLSI Design 2005: 730-735
2004		
27	EE	Victor Khomenko, Maciej Koutny, Alexandre Yakovlev: Logic Synthesis for Asynchronous Circuits Based on Petri Net Unfoldings and Incremental SAT. ACSD 2004: 16-25
26	EE	Fei Xia, Fei Hao, Ian G. Clark, Alexandre Yakovlev, E. Graeme Chester: Buffered Asynchronous Communication Mechanisms. ACSD 2004: 36-46
25	EE	Danil Sokolov, Julian Murphy, Alexandre V. Bystrov, Alexandre Yakovlev: Improving the Security of Dual-Rail Circuits. CHES 2004: 282-297
24	EE	Frank P. Burns, Delong Shang, Albert Koelmans, Alexandre Yakovlev: An Asynchronous Synthesis Toolset Using Verilog. DATE 2004: 724-725
23		Fei Hao, Fei Xia, E. Graeme Chester, Alexandre Yakovlev, Ian G. Clark: MATLAB Models of ACMS in Control Systems. ICINCO (3) 2004: 54-61
22	EE	D. J. Kinniment, Alexandre Yakovlev: Low Latency Synchronization Through

		Speculation. PATMOS 2004: 278-288
21	EE	Delong Shang, Frank P. Burns, Alexandre V. Bystrov, Alexandre V. Koelmans, Danil Sokolov, Alexandre Yakovlev: A Low and Balanced Power Implementation of the AES Security Mechanism Using Self-Timed Circuits. PATMOS 2004: 471-480
20	EE	Alexandre Yakovlev, Stephen B. Furber, René Krenz, Alexandre V. Bystrov: Design and Analysis of a Self-Timed Duplex Communication System. IEEE Trans. Computers 53(7): 798-814 (2004)
		2003
19	EE	Victor Khomenko, Maciej Koutny, Alexandre Yakovlev: Detecting State Coding Conflicts in STG Unfoldings Using SAT. ACSD 2003: 51-60
18	EE	Alexandre V. Bystrov, Danil Sokolov, Alexandre Yakovlev: Low-Latency Contro Structures with Slack. ASYNC 2003: 164-173
17	EE	Nikolai Starodoubtsev, Sergei Bystrov, Alexandre Yakovlev: Monotonic Circuits with Complete Acknowledgement. ASYNC 2003: 98-108
16	EE	Agnes Madalinski, Alexandre V. Bystrov, Victor Khomenko, Alexandre Yakovlev: Visualization and Resolution of Coding Conflicts in Asynchronous Circuit Design. DATE 2003: 10926-10931
15	EE	Danil Sokolov, Alexandre V. Bystrov, Alexandre Yakovlev: STG Optimisation in the Direct Mapping of Asynchronous Circuits . DATE 2003: 10932-10939
14	EE	Josep Carmona, Jordi Cortadella, Victor Khomenko, Alexandre Yakovlev: Synthesis of Asynchronous Hardware from Petri Nets. Lectures on Concurrency and Petri Nets 2003: 345-401
		2002
13		Jordi Cortadella, Alexandre Yakovlev, Grzegorz Rozenberg: Concurrency and Hardware Design, Advances in Petri Nets Springer 2002
12	EE	Jordi Cortadella, Alexandre Yakovlev, Jim D. Garside: T8: Logic Design of Asynchronous Circuits. ASP-DAC 2002: 26-30
11	EE	Alexandre V. Bystrov, Alexandre Yakovlev: Asynchronous Circuit Synthesis by Direct Mapping: Interfacing to Environment. ASYNC 2002: 127-136
10	EE	D. J. Kinniment, O. V. Maevsky, G. Russell, Alexandre Yakovlev, Alexandre V. Bystrov: On-Chip Structures for Timing Measurements and Test. ASYNC 2002: 190-
9	EE	Alexandre V. Bystrov, Maciej Koutny, Alexandre Yakovlev: Visualization of Partial Order Models in VLSI Design Flow. DATE 2002: 1089
8	EE	Victor Khomenko, Maciej Koutny, Alexandre Yakovlev: Detecting State Coding Conflicts in STGs Using Integer Programming. DATE 2002: 338-345
7	EE	Alexandre Yakovlev: Is the Die Cast for the Token Game? ICATPN 2002: 70-79
6		Agnes Madalinski, Alexandre V. Bystrov, Alexandre Yakovlev: Visualization of Coding Conflicts in Asynchronous Circuit Design. IWLS 2002: 155-160
5		Alexandre V. Bystrov, Alexandre Yakovlev: Synthesis of Asynchronous Circuits with Predictable Latency. IWLS 2002: 239-243
4	EE	Jordi Cortadella, Alexandre Yakovlev, Jim D. Garside: Logic Design of

		Asynchronous Circuits (Tutorial Abstract). VLSI Design 2002: 26-
3	EE	Fei Xia, Alexandre Yakovlev, Ian G. Clark, Delong Shang: Data Communication in Systems with Heterogeneous Timing. IEEE Micro 22(6): 58-69 (2002)
2001		
2	EE	Alexandre Yakovlev, Fei Xia, Delong Shang: Synthesis and Implementation of a Signal-Type Asynchronous Data Communication Mechanism. ASYNC 2001: 127-
1		Alan Burns, Andy J. Wellings, Frank P. Burns, Albert Koelmans, Maciej Koutny, Alexander B. Romanovsky, Alexandre Yakovlev: Modelling and verification of an atomic action protocol implemented in Ada. Comput. Syst. Sci. Eng. 16(3): 173-182 (2001)

The above listing includes 16 duplicates (on account of 13 articles co-authored by two or more members of the Committee), as follows.

2004: 9 duplicates
[Cor22] = [Lav33] = [Sot7]
[Cor20] = [Lav31] = [Sot5]
[Cor19] = [Lav29] = [Sot3]
[Edw4] = [Sot4]
[Gin5] = [Sot6]
[Hee2] = [Pig11]

2003: 2 duplicates
[Cor15] = [Lav26]
[Cor13] = [Yak14]

2002: 4 duplicates
[Cor12] = [Yak13], edited work that includes [Jos2] and [Var3]
[Cor11] = [Yak12]
[Cor7] = [Lav13]
[Cor5] = [Yak4]

2001: 1 duplicate
[Pig1] = [Ren2]

Besides the duplicates, there are several articles, e.g. [Yak20] = [Fur9] below, that are joint publications between members of ACiD-WG, though they have been co-authored by the representative of only one of them.

Furber (UoM)

2004		
12	EE	W. J. Bainbridge, L. A. Plana, Stephen B. Furber: The Design and Test of a Smartcard Chip Using a CHAIN Self-Timed Network-on-Chip. DATE 2004: 274-279
11	EE	Yijun Liu, Stephen B. Furber: The design of a low power asynchronous multiplier. ISLPED 2004: 301-306

10	EE	Yijun Liu, Stephen B. Furber: Minimizing the Power Consumption of an Asynchronous Multiplier. PATMOS 2004: 289-300
9	EE	Alexandre Yakovlev, Stephen B. Furber, René Krenz, Alexandre V. Bystrov: Design and Analysis of a Self-Timed Duplex Communication System. IEEE Trans. Computers 53(7): 798-814 (2004)
		2003
8	EE	W. J. Bainbridge, W. B. Toms, Doug Edwards, Stephen B. Furber: Delay-Insensitive, Point-to-Point Interconnect Using M-of-N Codes. ASYNC 2003: 132-140
7	EE	Z. C. Yu, Stephen B. Furber, L. A. Plana: An Investigation into the Security of Self-Timed Circuits. ASYNC 2003: 206-215
		2002
6	EE	Daranee Hormdee, Jim D. Garside, Stephen B. Furber: An Asynchronous Victim Cache. DSD 2002: 4-11
5	EE	Stephen B. Furber: Validating the AMULET Microprocessors. Comput. J. 45(1): 19-26 (2002)
4	EE	John Bainbridge, Stephen B. Furber: Chain: A Delay-Insensitive Chip Area Interconnect. IEEE Micro 22(5): 16-23 (2002)
		2001
3	EE	W. J. Bainbridge, Stephen B. Furber: Delay Insensitive System-on-Chip Interconnect using 1-of-4 Data Encoding. ASYNC 2001: 118-126
2	EE	P. A. Riocreux, L. E. M. Brackenbury, M. Cumpstey, Stephen B. Furber: A Low-Power Self-Timed Viterbi Decoder. ASYNC 2001: 15-24
1	EE	Stephen B. Furber, Aristides Efthymiou, Jim D. Garside, David W. Lloyd, Mike J. G. Lewis, Steve Temple: Power Management in the Amulet Microprocessors. IEEE Design & Test of Computers 18(2): 42-52 (2001)

Appendix 2 – Publications at ASYNC by Members

The following abstracts were obtained from http://www.computer.org/proceedings/cps_dl.htm, the IEEE Computer Society Digital Library.

11th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'05), March 14 - 16, 2005, New York City, New York, USA	
pp. 34-43 A Scheduling Discipline for Latency and Bandwidth Guarantees in Asynchronous Network-on-Chip Tobias Bjerregaard, Jens Sparsø (**DTU**) ***Best Paper Award***	Guaranteed services (GS) are important in that they provide predictability in the complex dynamics of shared communication structures. This paper discusses the implementation of GS in asynchronous Network-on-Chip. We present a novel scheduling discipline called Asynchronous Latency Guarantee (ALG) scheduling, which provides latency and bandwidth guarantees in accessing a shared media, e.g. a physical link shared between a number of virtual channels. ALG overcomes the drawbacks of existing scheduling disciplines, in particular the coupling between latency and bandwidth guarantees. A 0.12 µm CMOS standard cell implementation of an ALG link has been simulated. The operation speed of the design was 702 MDI/s.
pp. 44-53 An Asynchronous Router for Multiple Service Levels Networks on Chip Dobkin Rostislav, Victoria Vishnyakov, Eyal Friedman, Ran Ginosar (**Technion**)	Networks on Chip that can guarantee Quality of Service (QNoC) are based on special routers that can support multiple service levels. GALS SoCs call for asynchronous NoC implementations, to eliminate the need for synchronization when crossing clock domains. An asynchronous multi-service level QNoC router is investigated. It comprises multiple interconnected input and output ports, and arbitration mechanisms that resolve any output port and service level conflicts. Buffering and credit based transport are enabled, enhancing throughput. A synchronous and an asynchronous routers have been designed, and their performance is compared. The asynchronous router requires less area and enables a higher data rate.
pp. 54-63 An Asynchronous NOC Architecture Providing Low Latency Service and Its Multi-Level Design Framework E. Beigné, F. Clermidy, P. Vivet (CEA-LETI) A. Clouard (**ST**) M. Renaudin, (**INPG-**	The demands of scalable, low latency and power efficient System-On-Chip interconnect cannot only be satisfied by point-to-point or shared-bus interconnects. In this paper, we propose a new Asynchronous Network-On-Chip (NOC) architecture which provides low latency transfers. This architecture is implemented as a GALS system, where chip units are built as synchronous islands, connected together using a Delay Insensitive asynchronous Network-on-Chip topology. The proposed NOC protocol and its asynchronous implementation are presented as well as the multi-level modeling approach using SystemC language and Transaction-Level-Modeling. Preliminary simulation

TIMA)	results show that the Asynchronous NOC can offer 5 Gbytes/s throughput in a 0.13um CMOS technology.
pp. 66-75 Register Communication between Mutually Asynchronous Domains Joep Kessels (**Philips Research**)	We present the design of several so-called communication registers, which are modules that support non-blocking communication between two mutually asynchronous domains. For that purpose a communication register offers two mutually asynchronous access ports: a write and a read port. Communication registers differ from buffers in that read and write accesses are never held up. Consequently, data may get duplicated or lost. A read access, however, always delivers a value written into the register, although not necessarily the latest one. Each of the two access ports is either clocked or self-timed, where the accesses through a self-timed port are controlled by handshakes. Therefore, one can distinguish four different kinds of modules: one for each possible access port combination. For all four cases we give simple designs, which in several cases are subsequently refined to meet additional requirements, such as setting an upper-bound to the mutual timing interference, keeping the power consumption low, or reducing the latency.
pp. 76-85 Request-Driven GALS Technique for Wireless Communication System Miloš Krstic, Eckhard Grass (**IHP**) Christian Stahl (Humboldt Universität)	A Globally Asynchronous - Locally Synchronous (GALS) technique for application in wireless communication systems is proposed and evaluated. The GALS wrappers are based on a request-driven operation with an embedded time-out function. A formally verified GALS wrapper is deployed for the 'GALSification' of a baseband processor for WLAN. Details of the GALS partitioning, implementation and the design-flow are discussed. Furthermore, a test strategy based on built-in self-test (BIST) is suggested. The described baseband processor was fabricated and successfully tested. The GALS design is compared with a clock-gated, synchronous version. Advantages for system integration are achieved along with a 1% reduction in dynamic power consumption, a 30% reduction in peak power supply current, and 5 dB reduction in spectral noise.
pp. 86-96 Self-Timed Circuitry for Global Clocking Scott Fairbanks, Simon Moore (**UCam-CLab**)	We present an apparatus used to distribute a timing reference or clock across the extent of a digital system. Self-timed circuitry both generates and distributes a clock signal, while using less power and less skew compared to a clock tree. HSpice simulations in a 180nm CMOS process comparing the Distributed Clock Generator presented in this paper and an H-tree clock distribution system, each clocking a 16mm × 16mm area suggests a 30% power savings. Also worst

	case skew was reduced from 27ps to 2ps while using a clock period equivalent to 9 FO4 gates.
pp. 109-115 Controlling Event Spacing in Self-Timed Rings V. Zebilis, C. P. Sotiriou (**ICS-FORTH**)	Prior research in event spacing has identified two effects which contribute to the phenomenon of bursting events in self-timed systems, namely the Charlie and the Drafting effects. In this paper we attempt to further the understanding of these effects by presenting an analysis of their magnitude for a range of asynchronous handshaking controller implementations. The main contribution of this work is to demonstrate that event spacing irregularities are not an inherent property of self-timed circuits, but can be controlled by careful circuit design. We demonstrate that bursting effects are indeed dependent on the specific implementation of the handshaking circuits used in an asynchronous system, by showing that the magnitude of the Charlie and Drafting effects is implementation-dependent. We also explain how both of these effects can be mitigated by altering the electrical characteristics of the circuit implementation.
pp. 166-175 A Multiplexor Based Test Method for Self-Timed Circuits Frank te Beest, Ad Peeters (**Philips Research**)	A new test method for self-timed circuits is presented that only uses multiplexers to make the majority of combinational feedback loops testable. Combinational feedback loops are problematic for testing, since they introduce sequential behavior in a circuit. Traditionally feedback loops are broken with scan latches or even scan flip-flops, which causes not only a large area overhead, but also have a large impact on performance. The method we present significantly reduces the cost of testing a self-timed circuit, while it retains all the benefits of traditional scan test methods. Most importantly, the method remains fully compatible with standard combinational test pattern generation tools and provides up to 100% stuck-at fault coverage. With the presented test method it becomes cost effective to use scan test for a self-timed circuit without the need to add new specialized cells to a standard cell library.
10th International Symposium on Asynchronous Circuits and Systems (ASYNC'04), April 19 - 23, 2004, Crete, Greece	
pp. 41-50 Analog Micropipeline Rings for High Precision Timing Scott Fairbanks, Simon Moore (**UCam-CLab**)	I use asynchronous FIFO stages that are connected in rings to generate and deliver highly precise timing signals. I introduce a Micropipeline FIFO control stage that oscillates at frequencies greater to that found in a ring of three unloaded inverters. Tokens spread evenly through FIFO rings built from this control under certain conditions. The tokens are ‘locked’ into an equally separated pattern by a classical feedback control where the actuator is the FIFO control stage. The actuating variable is the stage latency which varies according to the temporal separation of its inputs. When the tokens

	in the FIFO ring are equally spaced, the relative phases of the nodes in the system assume predictable values. This technique allows the division of a better than three gate delay cycle time into an arbitrarily large number of phases whose precision is limited only by the limits of the fabrication process and noise. Applications that need a precise time reference can benefit from this technique. A/D conversion, clock recovery, and multi-phase clocking solutions are briefly sketched.
pp. 149-158 Handshake Protocols for De-Synchronization I. Blunno (**PoliTo**) J. Cortadella (**UPC**) A. Kondratyev (Cadence Berkeley Labs) L. Lavagno (**PoliTo** and Cadence Berkeley Labs) K. Lwin (Cadence Berkeley Labs) C. Sotiriou (**ICS-FORTH**) ***Best Paper Award***	De-synchronization appears as a new paradigm to automate the design of asynchronous circuits from synchronous netlists. This paper studies different protocols for de-synchronization and formally proves their correctness. A taxonomy of existing protocols for latch controllers is provided. In particular, four-phase handshake protocols devised for micro-pipelines are studied. A new controller with maximum concurrency for de-synchronization is also proposed. The applicability of de-synchronization on an implementation of the DLX microprocessor is also described and discussed.
pp. 170-180 Data Synchronization Issues in GALS SoCs Rostislav Dobkin, Ran Ginosar, (**Technion**) Christos P. Sotiriou (**ICS-FORTH**)	Locally generated, arbitrated clocks for GALS SoCs face the risk of synchronization failures if clock delays are not accounted for. The problem is analyzed based on clock delays, cycle times, and complexity of the asynchronous port controllers. A number of methods are presented. In some cases, it is sufficient to extract all the delays and verify whether the system is susceptible to metastability. In other cases, when high data bandwidth is not required, asynchronous synchronizers or matched-delay asynchronous ports may be employed. Arbitrated clocks may be traded off for locally delayed input and output ports, facilitating high data rates. The latter circuits have been simulated, to verify their performance.
p. 183 Bringing Handshake Technology to the Open Market Ad Peeters (**Philips Research**) *Keynote*	There are many incentives to tackle the chaos of asynchronous circuit technology. The holy grail of supreme speed is certainly one of them, but it remains a distant goal. However, today's market suffers from other problems for which asynchronous circuits may provide immediate answers - problems such as energy consumption and the integration of analog and digital circuits. Solutions in these domains may have direct impact on the market in areas such as automotive, wireless connectivity, identification and smart cards.

	A Line of Business within the Philips Technology Incubator, Handshake Solutions brings Handshake Technology to the semiconductor market. Handshake Technology is an extremely disciplined asynchronous design style, supported by a complete tool set for design, simulation, prototyping and testing. It enables the industrialization of asynchronous design and has been used in dozens of different IC types with tens of millions of ICs already sold with Handshake Technology inside.
pp. 198-206 Asynchronous FIR Filters: Towards a New Digital Processing Chain F. Aeschlimann, E. Allier, L. Fesquet, M. Renaudin (**INPG-TIMA**)	This paper is a contribution to the definition of a new kind of digital signal processing chain. It is focused on Finite-Impulse-Response filtering (FIR) applied to irregularly sampled signals obtained from an asynchronous analog to digital converter. The paper first formalizes the convolution operator in the irregular sampling context. The computational complexity is deduced and compared to the one of standard synchronous FIR filters. It shows that a significant reduction of the computational complexity is achievable, hence a reduction in terms of energy. The paper then describes the architecture of the asynchronous filter. It finally reports the simulations performed on a speech application, resulting in a reduction of the processing power of about one order of magnitude.
pp. 207-215 An Asynchronous, Iterative Implementation of the Original Booth Multiplication Algorithm A. Efthymiou, W. Suntiamorntut, J. Garside, L. E. M. Brackenbury (**UoM**)	One of the main reasons for using asynchronous design is that it offers the opportunity to exploit the data-dependent latency of many operations in order to achieve low-power, high-performance, or low area. This paper describes a novel, asynchronous, iterative multiplier which exhibits data-dependency in both the number of iterations required to produce the result and in the delay of each step of the iteration. The preliminary evaluation of the multiplier, implemented using standard-cells, shows that speed improvements can be achieved in comparison to a standard iterative, radix-4 Booth multiplier.
Ninth International Symposium on Asynchronous Circuits and Systems (ASYNC'03), May 12 - 15, 2003, Vancouver, B.C., Canada	
pp. 46-55 Adaptive Pipeline Structures for Speculation Control Aristides Efthymiou, Jim D. Garside (**UoM**)	Pipelining is a common method for improving the throughput of a system, especially when the majority of the processing is sequential. Unfortunately when the sequentiality is broken, a pipelined system suffers additional delay and, most importantly for this work, energy waste which is roughly proportional to the pipeline depth. Standard pipelines cannot be modified once they are built so their depth is fixed. This paper proposes a method that allows the dynamic adaptation of the structure of an asynchronous pipeline, so that

	pipeline stages can be merged and split at run-time, allowing greater flexibility. It is based on novel latch controllers that can be configured dynamically as ‘normal ’or ‘collapsed ’, i.e. keeping their latches permanently transparent. Using these controllers a model of AMULET3 was designed that is capable of changing its pipeline depth dynamically when branches are anticipated, in order to alleviate the energy loss when the branch finally arrives.
pp. 68-77 Timing Measurements of Synchronization Circuits Yaron Semiat, Ran Ginosar (**Technion**)	A regular (two-flop) synchronizer and six multi-synchronous synchronizers are implemented on a programmable logic device and are measured. An experiment system and method for measuring synchronizers and metastable flip-flops are described. Two separate settling time constants are shown for a metastable flop, confirming earlier results of Dike and Burton. Clocking cross-talk between asynchronous clocks is demonstrated. The regular synchronizer is useful for communications between asynchronous clock domains, while the other synchronizers can provide higher bandwidth communications between multi-synchronous and mesochronous domains.
pp. 89-96 Fourteen Ways to Fool Your Synchronizer Ran Ginosar (**Technion**)	Transferring data between mutually asynchronous clock domains requires safe synchronization. However, the exact nature of synchronization sometimes eludes designers, and as a result synchronization circuits get "optimized" to the point where they do no longer operate correctly. This paper reviews a number of such cases, analyzes the causes of the errors, and offers a correct synchronizer circuit for each case. A correct two-flop synchronizer is presented. After discussing cases that avoid synchronization, the following synchronizers are reviewed: one flop, sneaky path, greedy path, wrong protocol, global reset, async clear, DFT leakage, pulse, slow-to-fast, metastability blocker, parallel and shared flop synchronizers.
pp. 98-108 Monotonic Circuits with Complete Acknowledgement Nikolai Starodoubtsev (Tokyo University of Social Welfare) Sergei Bystrov (Russian Academy of Science) Alex Yakovlev (**UNew**)	The paper studies a class of asynchronous circuits in which every signal transition on the inputs of every gate is acknowledged during the circuit operation. This property is called complete acknowledgement (CA) and it is considered here for circuits that consist of gates described by monotonic boolean functions only.In order to implement such circuits the standard CMOS designs of 2-input logic gates are modified by using an additional output for CA. The paper investigates the behavioral properties of monotonic CA (MCA) circuits and the feasibility of a behavioral specification to be refined to a CA-implementable form. The result of comparison of a number of CA realizations with their speed-independent counterparts produced by negative

	gate synthesis inspires optimism about the practicality of CA circuits. Being particularly robust to variations in technological parameters, e.g. the value and type of delay and switching thresholds, such circuits offer potential advantages for future CMOS designs.
pp. 121-130 An Analysis of Determinacy Using a Trace-Theoretic Model of Asynchronous Circuits Mark B. Josephs (**LSBU**)	Receptive process theory provides a semantic model for reasoning about nput/output-systems in general, and about the switching behaviour of asynchronous circuits in particular. As in the failures/divergences model of Hoare's CSP, nondeterministic behaviour, as might result from the use of arbiters and synchronizers, can be modelled. A new result is the identification of the class of deterministic receptive processes, which is closed under composition. The defining characteristic of the class is that the behaviour of its members can be adequately described using a traces/divergences model. The closure of the class is proved with respect to a binary, parallel composition operator which allows inputs to be forked isochronically to both components and which conceals those outputs of either component that are inputs to the other component. This result contrasts with CSP, in which determinacy is not preserved when events are concealed.
pp. 132-140 Delay-Insensitive, Point-to-Point Interconnect Using M-of-N Codes J. Bainbridge, W. B. Toms, D. A. Edwards, S. B. Furber (**UoM**)	m-of-n codes can be used for carrying data over self-timed on-chip interconnect links. Such codes can be chosen to have low redundancy, but the costs of encoding/decoding data is high. The key to enabling the cost-effective use of m-of-n codes is to find a suitable mapping of the binary data to the code. This paper presents a new method for selecting suitable mappings through the decomposition of the complex m-of-n code into an incomplete m-of-n code constructed from groups of smaller, simpler m-of-n and 1-of-n codes. The circuits used both for completion detection and for encoding/decoding such incomplete codes show reduced logic size and delay compared to their full m-of-n counter-parts. The improvements mean that the incomplete m-of-n codes become attractive for use in on-chip interconnects and network-on-chip designs.
pp. 164-173 Low-Latency Control Structures with Slack A. Bystrov, D. Sokolov, A. Yakovlev (**UNew**)	OR-causality , or weak precedence, is a way to increase performance of asynchronous circuit in on-chip interfacing, computation process control, early evaluation in data-flow structures, error-recovery etc. The difficulties in hazard-free implementation of OR-causality restricted its use to the simplest cases of merging. We advance this subject by introducing slack in the taxonomy of OR-causality, which allows latency

	reduction to be achieved in the context of highly pipelined operation. Petri net model and circuit structures are proposed for the bounded and "almost" unbounded merge cases. The specifics of data or control token stream merging are studied in a number of examples. Those show the applicability of the new merge constructs to a wide range of functional operators, including arithmetic, Boolean and threshold functions.
pp. 196-205 A New Class of Asynchronous A/D Converters Based on Time Quantization E. Allier, G. Sicard, L. Fesquet, M. Renaudin (**INPG-TIMA**)	This work is a contribution to a drastic change in standard signal processing chains. The main objective is to reduce the power consumption by one or two orders of magnitude. Integrated Smart Devices and Communicating Objects are application domains targeted by this work. In this context, we present a new class of Analog-to-Digital Converters (ADCs), based on an irregular sampling of the analog signal, and an asynchronous design. Because they are not conventional, a complete design methodology is presented. It determines their characteristics given the required Effective Number of Bits and the analog signal properties. It is shown that our approach leads to a significant reduction in terms of hardware complexity and power consumption. A prototype has been designed for speech applications, using the STMicroelectronics 0.18-µm CMOS technology. Electrical simulations prove that the Factor of Merit is increased by more than one order of magnitude compared to synchronous Nyquist ADCs.
pp. 206-215 An Investigation into the Security of Self-Timed Circuits Z. C. Yu, S. B. Furber, L. A. Plana (**UoM**)	Self-timed logic may have advantages for security-sensitive applications. The absence of clock, as reliable timing reference, makes conventional power analysis attacks more difficult. However, the variability of the timing of self-timed circuits is weakness that could be exploited by alternative attack techniques. This paper introduces methodology for the differential power analysis of self-timed circuits which does not rely upon clock signal. This methodology is used to investigate the security of self-timed, ARM-compatible processor designed specifically to explore the benefits of self-timed design in secure applications. Timing analysis is also applied to the same design. The results from the analyses are presented and confirm that self-timed logic with dual-rail encoding and secure storage significantly improves resistance to non-invasive attacks.
Eighth International Symposium on Asynchronous Circuits and Systems (ASYNC'02), April 08 - 11, 2002, Manchester, United Kingdom	
pp. 59-68	We present a method for synchronizing pausible clocks

Clock Synchronization through Handshake Signalling Joep Kessels (**Philips Research)** Suk-Jin Kim (Kwang-Ju Institute of Science and Technology**)** Ad Peeters, Paul Wielage (**Philips Research**)	in GALS (Globally Asynchronous, Locally Synchronous) systems. In contrast to most conventional GALS schemes the method is not based on including in each ring oscillator a synchronizing element (such as for instance an arbiter) which on one side can pause the clock and on the other side offers a handshake interface. Instead, we propose a scheme in which each synchronous module has both an incoming and an outgoing clock signal, which have been obtained by opening the module's ring oscillator. Since these clock signals also behave as handshake signals, handshake circuits can be used to synchronize the clocks. We demonstrate the technique in the context of processors and memories. All the designs have been simulated and showed functionally correct.
pp. 69-75 Point to Point GALS Interconnect Robert Mullins, George Taylor, Peter Robinson, Simon Moore (**UCam-CLab**)	Reliable, low-latency channel communication between independent clock domains may be achieved using a combination of lock pausing techniques, self-calibrating delay lines and an asynchronous interconnect. Such a scheme can be used for point-to-point communication in a globally asynchronous locally synchronous (GALS) system, a possible methodology for managing the predicted increase in clock domains. We present interface wrapper circuits which permit communication between a locally synchronous producer and a locally synchronous consumer via an asynchronous interconnect. Such interfaces can also be used to mix asynchronous and synchronous modules. Clock pausing is used to guarantee that metastability will never result in failure. Arbitration between channel communication and the local clock is performed concurrently so that metastability resolution will rarely delay the clock. Simulation results show that the maximum performance of one data item per consumer clock cycle is achieved when the producer:consumer clock ratio is equal or greater to one. This communication mechanism is suited to other asynchronous interconnect methods which offer low power and high performance.
pp. 76-83 A Dual-Mode Synchronous/Asynchronous CORDIC Processor Eckhard Grass, Bodhisatya Sarker, Koushik Maharatna (**IHP**)	For application in a software defined radio a CORDIC processor has been developed that can operate both in synchronous and asynchronous mode. Each mode of operation has advantages and drawbacks. Depending on the actual application, an optimal trade-off can be achieved by selecting the mode of operation that fits best with system demands. We believe that for a system developer this additional degree of freedom significantly increases the application space. The

	design has been implemented on a 0.25 micrometer SiGe:C BiCMOS process. Simulation results using post-layout extracted parameters indicate that the design is competitive both with purely synchronous and purely asynchronous implementations.
pp. 127-136 Asynchronous Circuit Synthesis by Direct Mapping: Interfacing to Environment Alex Yakovlev, Alexandre Bystrov (**UNew**)	Direct mapping helps avoid algorithmic complexity which is inherent in logic synthesis methods. However, existing techniques for direct mapping of Petri net specifications to asynchronous control circuit do not deliver in performance due to logic overhead and inefficient interface to the environment. The paper presents a direct mapping method for Signal Transition Graphs (STGs) targetted at lower latency between input and output events. It is based on two behaviour-preserving transformations applied to the initial STG model: output exposition and environment tracking. The former allows interface signals to be generated concurrently to internal transitions. The latter prevents creation of coding conflicts. Subsequent refinement combines the use of the tracking and input signals in the control of the output flip-flops so as to optimise the circuit size by removing some tracking components. The depth of final logic in the design examples is one or two gates. The comparison to logic synthesis methods indicates lower output latency and greater size. The proposed direct-mapping method allows using fast transistor-level implementations for tracking and output signals with well-localised relative timing constraints.
pp. 161-170 Adding Synchronous and LSSD Modes to Asynchronous Circuits Kees van Berkel (**Philips Research** and Eindhoven University of Technology) Frank de Beest (University of Twente) Ad Peeters (**Philips Research**)	A synchronous mode as well as a scan mode of operation are added to a large class of asynchronous circuits, in compliance with LSSD design rules. This enables the application of mainstream tools for design-for-testability and test-pattern generation to asynchronous circuits. The approach is based on a systematic transformation of all single-output sequential gates into synchronous and scannable versions. By exploiting dynamic circuit operation in scan mode, the overhead of this transformation in terms of both circuit cost and circuit delay is kept minimal.
pp. 190-197 On-Chip Structures for Timing Measurements and Test G. Russell, A. V. Yakovlev, A. Bystrov, D. J.	This paper describes the use of digitally set delay lines in conjunction with MUTEX time comparison circuits, to measure on-chip signal path timing differences to accuracies of better than 10ps. Three methods of time measurement are described. The first, which uses parallel MUTEXs with a tapped delay line, is analogous to a flash A/D converter. The second one is similar to a successive approximation method. Both are

Kinniment, O. V. Maevsky (**UNew**)	fast, and efficient, but the second requires less hardware for a large number of bits. The third technique uses a MUTEX to amplify small time differences to a measurable size. Applications for these techniques include adaptive synchronization and input tests, such as data set-up time conditions that currently require the use of very expensive test hardware. We describe an on-chip method of testing these conditions, using uncorrelated signals whose statistics are known, and accurately selecting the conditions to be tested on-chip.
pp. 201-210 SPA — A Synthesisable Amulet Core for Smartcard Applications W. J. Bainbridge, P. A. Riocreux, J. D. Garside, A. Bardsley, S. Temple, L. A. Plana (**UoM**)	SPA is a synthesised, self-timed, ARM-compatible processor core. The use of synthesis was mandated by a need for rapid implementation. This has proved to be very effective, albeit with increased cost in terms of area and performance compared with earlier non-synthesised processors. SPA is employed in an experimental smartcard chip which is being designed to evaluate the applicability of self-timed logic in security-sensitive devices. The Balsa synthesis system is used to generate dual-rail logic with some enhancements to improve security against non-invasive attacks. A complete system-on-chip is being synthesised with a only small amount of hand design being employed to boost the throughput of the on-chip interconnection system.
pp. 211-218 Improving Smart Card Security Using Self-Timed Circuits Paul Cunningham, Ross Anderson, Robert Mullins, George Taylor, Simon Moore (**UCam-CLab**)	We demonstrate how 1-of-n encoded speed-independent circuits provide a good framework for constructing smart card functions that are resistant to side channel attacks and fault injection. A novel alarm propagation technique is also introduced. These techniques have been used to produce a prototype smart card chip: a 16-bit secure processor with Montgomery modular exponentiator and smart card UART.
Seventh International Symposium on Asynchronous Circuits and Systems (ASYNC'01), March 11 - 14, 2001, Salt Lake City, Utah	
pp. 4-14 Exploiting Typical DSP Data Access Patterns and Asynchrony for a Low Power Multiported Register Bank M. Lewis (Ericsson Microelectronics AB) L. Brackenbury (**UoM**)	CADRE (Configurable Asynchronous Dsp for Reduced Energy) is a low-power asynchronous DSP (digital signal processor) architecture intended for digital mobile phone chipsets. Central to the architecture are the X and Y register banks, which supply the four processing units with the data they require and to which results are written. The register banks each require 10 read and 6 write ports to service all possible requests, leading to a large and power-hungry unit if implemented directly. Instead, typical DSP data access patterns are exploited to produce a partitioned design

	which offers fast and low-power operation in typical cases but also caters for worst-case patterns. Power consumption and performance results for the register bank with the DSP running typical algorithms are presented, and it is shown that the register bank consumes only 8% of total power (core and memory) in what is already a highly power-efficient system.
pp. 15-24 A Low-Power Self-Timed Viterbi Decoder P.A. Riocreux, L.E.M. Brackenbury, M. Cumpstey, S.B. Furber (**UoM**)	Viterbi decoders are used for decoding data encoded using convolutional forward error correction codes or data that suffers from inter-symbol interference. They occur in a large proportion of digital transmission and digital recording systems, including digital mobile telephony and digital TV broadcast, CD-ROM and magnetic disk reading. This paper describes a design for a self-timed Viterbi decoder. The new design is based upon serial, unary arithmetic for the manipulation and storage of metrics. In the trace-back system, multiple concurrent trace-backs may be running and trace-backs are terminated as soon as they cease to be useful. The new architecture occupies between 29% and 23% less area than a selection of synchronous implementations with the same design parameters which use the same process and cell-library.
pp. 25-34 A Multi-Radix Approach to Asynchronous Division Gianluca Cornetta, Jordi Cortadella (**UPC**)	The speed of high-radix digit-recurrence dividers is mainly determined by the hardware complexity of the quotient-digit selection function. In this paper we present a scheme that combines the area efficiency of bundled data with data-dependent computation time. In this scheme the selection function is very simple and may be implemented using a fast adder. This function speculates the result digit and, when the speculation is incorrect, a correction of the quotient and of the residual must be performed. When the residual satisfies some constraints it is also possible to switch to a higher radix, computing a fraction of the next digit in advance. This results in a division scheme with a variable iteration time and a variable number of iterations and hence with an asynchronous behaviour. Several designs were realized and compared both in terms of execution time and area. The fastest unit considered is a radix-64 divider that may switch to radix 128 or 256. Our evaluations show that area x delay savings from 25% to 65%, compared to equivalent synchronous designs, may be achieved.
pp. 36-45 A Practical Comparison of Asynchronous Design Styles	It is well known that single-rail, bundled-delay circuits provide good area efficiency but it can be difficult to match them with appropriate delay models. Conversely delay insensitive circuits such as those employing dual-rail codes are larger but it is easier to ensure timing correctness. In terms of speed, bundled-delay circuits

D.W. Lloyd (**ST**) J.D. Garside (**UoM**)	need conservative timing but dual-rail circuits can require an appreciable completion detection overhead. This paper compares designs in both of these styles and also a delay-insensitive 1-of-4 coded circuit using the practical example of an ARM Thumb instruction decoder. The results show that, through the application of careful optimizations, the 1-of-4 circuits out-performed single-rail circuits and reduced the power compared to dual-rail circuits.
pp. 86-95 Synchronous Handshake Circuits Ad Peeters, Kees van Berkel (**Philips Research**)	We present the synchronous implementation of hand-shake circuits as an extra feature in the otherwise asynchronous design flow based on Tangram. This synchronous option can be used in the mapping onto FPGAs or as a fall-back option to provide a circuit that is easier to test and integrate in a synchronous environment. When single-rail and synchronous realizations of the same handshake circuit are compared, the synchronous versions typically require fewer state-holding elements, occupy less area, have similar performance, but consume significantly more power (in the examples studied up to a factor four). Synchronous handshake circuits provide a means to study clock-gating techniques based on the synthesis starting from a behavioral-level specification. In addition, the study provides hints as to where the asynchronous hand-shake circuits may be optimized further.
pp. 108-117 Designing an Asynchronous Bus Interface Joep Kessels, Ad Peeters (**Philips Research**) Torsten Kramer (Kramer-Consulting) Markus Feuser, Klaus Ully (Philips Semiconductors)	By presenting the design of an asynchronous bus interface for the 80C51 microcontroller we show that non-channel communications are needed to come to a modular and efficient solution. We derive the bus design by applying five transformations to an initial design that is completely based on channel communications. In each of the steps we first discuss the problem to be solved. The final design uses both channel and non-channel communications, the latter kind of communications being based on shared variables. In principle, communicating through variables is less safe than communicating through channels. We propose so-called communication sessions to obtain safe communications through variables. Communication sessions are well-defined periods of time during which the access rights with respect to a set of variables are transferred from one activity to another. We also show that such sessions can be implemented using conventional channels.
pp. 118-126 Delay Insensitive System-on-Chip Interconnect using	The demands of System-on-Chip (SoC) interconnect increasingly cannot be satisfied through the use of a shared bus. A common alternative, using unidirectional, point-to-point connections and multiplexers, results in

1-of-4 Data Encoding W.J. Bainbridge, S.B. Furber (**UoM**)	much greater area requirements and still suffers from some of the same problems. This paper introduces a delay-insensitive, asynchronous approach to interconnect over long paths using 1-of-4 encoded channels switched through multiplexers. A re-implementation of the MARBLE SoC bus (as used in the AMULET3H chip) using this technique shows that it can provide a higher throughput than the simpler tristate bus while using a narrower datapath.
pp. 127-136 Synthesis and Implementation of a Signal-Type Asynchronous Data Communication Mechanism A. Yakovlev, F. Xia, D. Shang (**UNew**)	This paper describes the synthesis and hardware implementation of a signal-type asynchronous data communication mechanism (ACM). Such an ACM can be used in systems where a data-driven ("lazy") logic must be interfaced with a time-driven ("busy") environment. A new classification system for ACMs is introduced. The conceptual definition of the signal ACM (called simply "Signal") is refined using Petri net techniques. Based on this, a more precise, state graph specification of a two-slot Signal is then constructed. Using theory of regions, a Petri net specification of the ACM is synthesized from the state graph. The Petri net model is then translated into a hardware implementation, which is entered into Cadence tools. Simulation results show that the hardware does conform to the definitions and specifications. The techniques employed in this work are potentially useful in the development of an automated process of synthesising similar systems.